English Translation of Japanese Patent Laid-Open 61-234027
Published: October 18, 1986
Inventor(s): Kyoichi SUGURO

Translated: August 19, 1998

(19) JAPAN PATENT OFFICE (JP)
(12) PATENT PUBLICATION OFFICIAL REPORT(A)
(11) PATENT APPLICATION PUBLICATION NUMBER SHO61-234027
(43) PUBLICATION: October 18, 1986
(54) TITLE OF THE INVENTION: A METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE
(21) APPLICATION NUMBER: 60-74372
(22) FILING DATE: April 10, 1985
(72) INVENTOR: Kyoichi Suguro
Toshiba Comprehensive Research Institute
1, Komukai-toshiba-cho, Saiwai-ku, Kawasaki-shi
(71) APPLICANT: Director General
Agency of Industrial Science and Technology

Specification

1. Title of the Invention

A Method for Manufacturing A Semiconductor Device

2. Claims

(1) A method for manufacturing a semiconductor device for manufacturing a laminated MOS transistor, comprising a step for forming a flat insulation film on a lower layer transistor, a step for forming an opening portion on a source or a drain of the lower layer transistor of the above insulation film, a step for epitaxial growth of a metallic silicide at the opening portion of the above insulation film, a step for attaching a silicon film over the whole surface in super high vacuum below $1x10^{-3}$ torr, and for solid phase epitaxial growth of the above silicon film with the above metallic silicide as a seed, and a step for forming an upper layer transistor on the above silicon film after the above solid phase epitaxial growth.

(2) A method for manufacturing a semiconductor device set forth in claim 1, wherein the above metallic silicide is $NiSi_2$, $CoSi_2$, PtSi or Pd_2Si.

(3) A method for manufacturing a semiconductor device set forth in claim 1, wherein each of the above upper and lower layers an MOS transistor having conductive channels different to each other.

3. Detailed Description of the Invention

[Field of the Invention]

The present invention relates to a method for manufacturing a 3-

dimensional semiconductor device, more specifically, relates to a method for manufacturing a semiconductor device having a laminated transistor structure.

[Technical Background of the Invention and Problems]

In recent years, widely developed is what is called SOI (Silicon On Insulator) technology, wherein a silicon monocrystal layer is formed on an insulation film by annealing by use of an electronic beam or a laser beam. And examinations have been made on the manufacture of what is called 3-dimensional IC, wherein elements are formed in 3-dimensional manners by use of this SOI technology.

In the manufacture of a 3-dimensional IC, for example, a 2-layer structure element, an interlayer insulation film is formed on an element (lower layer element) formed on a monocrystal silicon substrate surface, thereafter a monocrystal silicon thin film whose direction is controlled by SOI technology is formed. And then, an element (upper layer element) is formed on the monocrystal silicon thin film.

However, in this kind of method, there have been the following problems. Namely, a silicon thin film for forming an upper layer element is formed by epitaxial growth with a monocrystal silicon substrate exposed to an opening portion arranged at an insulation film as a seed. When seeding epitaxy by beam annealing is used, it is necessary to make thick the under surface insulation film of a silicon thin film, and by this thick film formation, the difference in conditions to melt an SOI and a silicon thin film, which is upper seed portion, widens (SOI is more apt to be melted), as a consequence, process margin becomes narrow, and it is very difficult to form a laminated device having three layers or more.

Under such circumstances, a horizontal seeding epitaxy technology by solid epitaxial growth has been recently reported (Applied Physics Letters, volume 43, p.1028). According to the result thereof, it is said that a horizontal seeding epitaxy about 5 to 6μm (from a seed portion) occurs on an oxide film of 0.2μm. A problem with solid phase epitaxy method is that crystal defects are apt to occur at a seed end, i.e., at a step portion of oxide film. And when to actually form a laminated device by use of solid phase epitaxy, there will be the following problems.

When an upper layer element and a lower layer element are connected, by connecting the insides of elements, it is possible to make

small the area occupied by elements. However, in the case of a CMOS inverter, whose lower layer portion is N channel, while whose upper layer portion is P channel, when a type N diffusion layer and a type P diffusion layer are connected, mutual dispersion of impurities occurs in heating process, as a result, the contact property of a contact portion is deteriorated. To cope with such a problem, there may be a method wherein a metallic silicide which is stable at high temperature process is employed between a type N diffusion layer and a type P diffusion layer, but, since the metallic silicide is polycrystal, it is difficult to avoid the mutual dispersion of impurities. Further, the polycrystal property prevents a horizontal epitaxial growth from a seed portion, which in turn causes the deterioration of element characteristics in crystal grain boundary, and the unevenness in element characteristics.

[Object of the Invention]

The present invention has been made in consideration of the above problems, accordingly, one object of the present invention is to provide a method for manufacturing a laminated semiconductor device, that enables to obtain preferable contact characteristics at connection portion of upper and lower layers, and to prevent the deterioration of element characteristics and the unevenness of element characteristics owing to crystal grain boundary to the utmost.

[Outline of the Invention]

The gist of the present invention lies in that a silicon layer for formation of an upper layer element is formed by solid phase epitaxial growth, and an epitaxial metallic silicide arranged at an opening portion of an interlayer insulation film is employed as a seed portion of the growth layer.

Namely, the present invention may be embodied as a method for manufacturing a semiconductor device for manufacturing a laminated MOS transistor, comprising a step for forming a flat insulation film on a lower layer transistor, a step for forming an opening portion on a source or a drain of the lower layer transistor of the above insulation film, a step for epitaxial growth of a metallic silicide at the opening portion of the above insulation film, a step for attaching a silicon film over the whole surface in super high vacuum below $1x10^{-3}$ torr, and also the above silicon film is grown in the solid phase epitaxial growth with the above metallic silicide as a seed, and a step for forming an upper layer transistor on the above silicon film after the above solid phase epitaxial

growth.

[Effects of the Invention]

According to the present invention, since the epitaxial metallic silicide prevents the mutual dispersion of impurity atoms on upper and lower layers, it is possible to obtain a preferable contact between upper and lower layers. And further, because of a monocrystal silicon film formed stably by solid phase epitaxy, and a flat under surface insulation film, a high performance laminated transistor with reproducibility is realized.

[Description of Preferred Embodiment]

In reference to one preferred embodiment shown in the attached drawings, the present invention is explained in details hereinafter.

FIG.1 is a cross section showing an outline structure of a CMOS inverter according to one preferred embodiment under the present invention. On a Si substrate 11, formed are a gate oxide film 13 and a gate electrode 14, and further, impurity doping layers 15 and 17 to be source and drain areas are formed thereon, and thus an N channel lower layer MOS transistor is structured. On the lower layer MOS transistor, formed via interlayer insulation films 18 and 19, is a monocrystal silicon film 31 by solid phase epitaxial growth. And a gate oxide film 33 and a gate electrode 34 are formed on this silicon film 31, and further, impurity doping layers 35 and 37 to become source and drain areas are formed thereon, and thus a P channel upper layer MOS transistor is formed. And one of the source drain of these MOS transistors is connected to an $NiSi_2$ film 21 by epitaxial growth. By the way, the reference numerals 12 and 32 show oxide films for separating elements, while 16 and 36 show side wall oxide films.

FIG.2 (a) through FIG.2(d) are cross sections showing manufacture processes of the above inverter. First, as shown in FIG.2 (a), an oxide film 12 for separating elements of thickness 0.4μm was formed on a P type Si substrate 11 of plane direction 100, and ratio resistance 5Ω/cm. Thereafter, a gate oxide film 13 of thickness 100Å and a tungsten gate 14 of width 1μm and thickness 0.2μm were formed by use of CVD method, $1x10^{14}$ cm^{-2} of As is ion implemented at 20 KeV, and thereby a shallow doping layer 15 was formed. Thereafter, by the side wall left technology well known conventionally, a side wall oxide film 16 was formed, and further, $3x10^{15}$ cm^{-2} of As is ion implemented at 80 KeV, and thereby a deep doping layer 17 was formed. Thereby, an N channel

under layer MOS transistor comprising a gate oxide film 13, a gate electrode 14 and an impurity doping layer 17 is configured.

In the next place, as shown in FIG.2 (b), by use of CVD method, an oxide film 18 of thickness 0.2μm and an oxide film 19 by bias spatter method were attached, thereafter, the surface of an oxide film 19 was flattened by use of resist etch back method. Thereafter, an opening portion 20 was formed on a drain 17 of under layer transistor.

In the next place, as shown in FIG.2 (c), by use of MBE method, in super high vacuum of $1x10^{-10}$ torr, an $NiSi_2$ film (metallic silicide) of thickness 1.5μm was formed all over the surface. thereafter, $NiSi_2$ film 21 after epitaxial growth by use of resist etch back method was etched, and the film 21 was left only in the opening portion 20. Namely, an embedded $NiSi_2$ film 21 was formed on the opening portion 20.

Thereafter, as shown in FIG.2 (d), a silicon film 31 of thickness 0.4μm was attached on the whole surface in vacuum of $1x10^{-10}$ torr, and with substrate temperature at 300°C, thereafter, heating process was carried out at temperature 620°C for 10 hours. This heating process causes epitaxial growth of the silicon film 31 about 6μm in horizontal direction from the embedded $NiSi_2$ film 21.

The latter processes were same as in the case to manufacture a lower layer transistor, and a P channel upper layer MOS transistor comprising a gate oxide film 33, a gate electrode 34 and impurity doping layers 35 and 37 were manufactured, and thus a CMOS inverter as shown in FIG.1 is completed.

As mentioned heretofore, according to the present preferred embodiment, a silicon film 31 for forming an upper layer transistor is formed by solid phase epitaxial growth, different from the case using beam anneal method, there is nor fear of occurrence of difference in silicon melting conditions at SOI portion and seed portion, and it is possible to take a large process margin, thus it is extremely effective for manufacture of laminated devices. And further, $NiSi_2$ film 21 at seed portion is formed by epitaxial growth, so even in the case with different conductive types in connection portion of upper and lower layers such as in a CMOS inverter, the mutual dispersion of impurities is extremely scarce. Therefore, it is possible to obtain preferable contact characteristics between upper and lower layers connections. And moreover, the surface of an oxide film 19 to be an interlayer insulation

film is flattened, so it is possible to obtain stable characteristics of upper layer transistor. Herein, if the surface of the oxide film 19 is not flattened, gate length becomes 2μm or less, and in the case of discrepancy of gate positions of upper and lower layers transistors, it is not possible to obtain stable characteristics of upper layer transistor.

By the way, the present invention is not limited solely to the above preferred embodiment. For example, the metallic silicide to be formed at the opening portion of the above interlayer insulation film is not limited to $NiSi_2$, but $CoSi_2$, PtSi, Pd_2Si, and other metallic silicide by epitaxial growth may be employed. And the conductive channels of each transistor of upper and lower layers may be reverse, which is of course well understood by those skilled in the art. And further, the present invention is not solely applied to a CMOS inverter, but may be applied to the manufacture of various types of laminated MOS devices. And as an Si substrate, an Si substrate through epitaxial growth may be employed. Thereby laminated structure elements of three layers or more are realized. Additionally, it is possible to arrange in various ways within the range of the gist of the present invention.

4. Brief Description of the Drawings

FIG.1 is a cross section showing an outline structure of a CMOS inverter according to one preferred embodiment under the present invention. FIG.2 (a) through FIG.2(d) are cross sections showing manufacture processes of the above inverter.

11 ... Si substrate
12, 32 ... Oxide film for separating elements
13, 33 ... gate oxide film
14, 34 ... Gate electrode
15, 35 ... Shallow doping layer
16, 36 ... Side wall oxide film
17, 37 ... Deep doping layer
18, 19 ... Interlayer insulation film
20 ... Opening portion
21 ... $NiSi_2$ film (metallic silicide)
31 ... Silicon film